

Laboratory 4

CS 210
Winter 2004
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Construct circuits that implement the following flip-flops using only NOR and AND gates. Test the circuits at clock frequencies .25 Hz, 1 Hz and 4 Hz.

- 1 A clocked RS flip-flop.
- 2 A clocked D flip-flop.
- 3 A clocked JK flip-flop.
- 4 A clocked T flip-flop.

For each circuit you construct, include the following information:

- The name of the circuit.
- A logic diagram, including
 - input variables
 - output names
 - Standard symbols for NOR and AND gates
 - Connecting wires
- A Minimized characteristic expression for circuit outputs Q_{t+1} and Q'_{t+1} at time $t+1$, in terms of Q_t at time t and the circuit inputs.