

Laboratory 3

CS 210
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The following are taken from lab exercise 11-7, chapter 11 of Mano, "Digital Design."

- 1 Construct a circuit that implements a 1-bit half adder using XOR and NAND gates.
- 2 Construct a circuit that implements a 1-bit full adder using XOR and NAND gates.
- 3 Construct a circuit that implements a 4-bit binary full adder-subtractor with a mode select input (see Figure 11-11) using a 4-bit binary full adder and XOR gates. In the truth table, only show output values w.r.t. truth assignments in which inputs $A_4A_3A_2A_1$ are assigned 1001.
- 4 Construct a circuit that implements a 4-bit magnitude comparator having three outputs x , y and z .

if $A_4A_3A_2A_1 = B_4B_3B_2B_1$, $x = 1$; otherwise, $x = 0$.

if $A_4A_3A_2A_1 < B_4B_3B_2B_1$, $y = 1$; otherwise, $y = 0$.

if $A_4A_3A_2A_1 > B_4B_3B_2B_1$, $z = 1$; otherwise, $z = 0$.

Use the adder-subtractor constructed in problem 3, inverters and AND gates. In the truth table, only show output values w.r.t. truth assignments in which inputs $A_4A_3A_2A_1$ are assigned 1001.