

Laboratory 5

CS 210
Fall 1999
Craig A. Rich

Construct sequential circuits which implement the following state diagrams using JK flip-flops. Test the circuits at clock frequency 1 Hz.

1 Multiple-of-3 recognizer:

$$y = \begin{cases} 1, & \text{if the sequence of inputs } x \text{ is a multiple of 3;} \\ 0, & \text{otherwise.} \end{cases}$$

2 2-bit up-down counter with an enable (E) and mode select (M) input:

$$E = \begin{cases} 1, & \text{enable incrementing or decrementing;} \\ 0, & \text{disable incrementing and decrementing.} \end{cases}$$
$$M = \begin{cases} 1, & \text{state is incremented (if enabled);} \\ 0, & \text{state is decremented (if enabled).} \end{cases}$$

For each sequential circuit which you construct, include the following information:

- The name of the circuit.
- A state table showing present state, circuit inputs, circuit outputs, next state, and flip-flop inputs (according to the flip-flop excitation table).
- A Karnaugh map and minimized Boolean expression for each circuit output and flip-flop input.
- A logic diagram, including
 - Symbols for NAND, NOR, inverter, AND, OR, exclusive OR gates enclosed within dashed rectangle(s) representing the IC chip(s) which contain the gates.
 - Block diagrams for flip-flops
 - Connecting wires labeled at either end with pin numbers, input variables, and/or output names.
- Observations and conclusions.